- - REMARKS - -

The present amendment replies to a First Non-Final Office Action dated June 5, 2002. Claims 1-15 are currently pending in the present application. Claims 1-15 have been amended herein to correct format errors. Attached hereto is a marked-up version of an amendment to claims 1-15 that is captioned "**Version With Markings To Show Changes Made**". No new matter has been introduced by the amendment of claims 1-15.

The Applicant is concurrently filing a marked-up specification and a substitute specification in accordance with 37 CFR §1.125. No new matter was introduced into the substitute specification.

In the First Non-Final Office Action, Examiner Tran objected to and rejected pending claims 1-15 on various grounds. The Applicant responds to each objection and rejection as subsequently recited herein, and respectfully requests reconsideration and further examination of the present application under 37 CFR § 1.112:

A. Claims 9 and 15 were rejected under 35 U.S.C. §112, ¶2 as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention

Claim 9 has been further amended to omit "as far as depending on claim 7", and claim 15 has been further amended to depend from claim 1. Withdrawal of the rejection of claims 9 and 15 under 35 U.S.C. §112, ¶2 as being indefinite is therefore respectfully requested.

B. Claim 15 was objected to under 37 C.F.R. §1.75(c) as being in improper form as a multiple dependent claim depending upon other multiple dependent claims

Claim 15 has been further amended to depend exclusively from claim 1. Withdrawal of the objection of claim 15 under 37 C.F.R. §1.75(c) as being in improper form is therefore respectfully requested.

C. Claims 1, 2, 10, 12 and 13 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,847,586 to *Burstein* et al.

The Applicant has thoroughly considered Examiner Tran's remarks concerning the patentability of independent claim 1 over *Burstein*. The Applicant has also thoroughly read *Burstein*. To warrant this §102(b) rejection, *Burstein* must show each and every limitation of independent claim 1 in as complete detail as is contained in claims 1 and 5. See, MPEP 2131. The Applicant respectfully traverses this 35 U.S.C. §102(b) rejection of claim 1, because *Burstein* unequivocally does not disclose, teach or suggest a comparator device "arranged for comparing the currents received at its two current inputs (11, 12) and for generating at the measuring signal output (13) a measuring signal (S) with a first value when the current received at its second current input (12) is less than the current received at its first current input (11), and with a second value when the current received at its second current input (12) is more than the current received at its first current input (11)" as recited in independent claim 1.

Specifically, Examiner Tran mistakenly reads *Burstein* as disclosing a comparator device in the form of a node POR that receives two currents and generates an output when one current is less or more than the other. As is well known in the art, a comparator provides an output with a magnitude of either a first value or a second value, the actual value being a function of a comparison of the inputs. However, a proper reading of *Burstein* clearly reveals that *Burstein* did not disclose, teach or suggest the node POR as a comparator device.

First, *Burstein* does not disclose, teach or suggest a magnitude of the output at node POR as a function of a comparison of the two currents. Second, as illustrated in FIGS. 4 and 8, *Burstein* teaches the magnitude of the output at node POR increases from zero (0) volts to a VDC trip level as the supply voltage increases from zero (0) volts to approximately 2.3 volts. Moreover, *Burstein* further teaches the output at node POR varies between zero (0) volts and three (3) volts for a supply voltage of three (3) volts as illustrated in FIG. 5, and the output at node POR varies between zero (0) volts and five (5) volts for a supply voltage of five (5) volts as illustrated in FIGS. 6 and 9.

Consequently, the output a node POR could have one of many values whenever one current is greater than the other, and vice-versa. A comparator as known in the art does not operate in this manner. This clearly demonstrates that *Burstein* did not intend to use the node POR as a comparator. Thus, *Burstein* fails to disclose, teach or suggest the magnitude of the output at the node POR having " a first value when the current received at its second current input (12) is less than the current received at its first current input (11)" and "a second value when the current received at its second current input (12) is more than the current received at its first current input (11)" as recited in independent claim 1.

Withdrawal of the rejection of independent claim 1 under 35 U.S.C. §102(b) as being anticipated by *Burstein* is therefore respectfully requested.

Claims 2, 10, 12 and 13 depend from independent claim 1. Therefore, dependent claims 2, 10, 12 and 13 include all of the elements and limitations of independent claim 1. It is therefore respectfully submitted by the Applicant that dependent claims 2, 10, 12 and 13 are allowable over *Burstein* for at least the same reason as set forth with respect to independent claim 1. Withdrawal of the rejection of dependent claims 2, 10, 12 and 13 under 35 U.S.C. §102(b) as being anticipated by *Burstein* is therefore respectfully requested.

D. Claim 8 was rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,847,586 to *Burstein* et al.

Claim 8 depends from independent claim 1. Therefore, dependent claim 8 includes all of the elements and limitations of independent claim 1. It is therefore respectfully submitted by the Applicant that dependent claim 8 is allowable over *Burstein* for at least the same reason as set forth with respect to independent claim 1. Withdrawal of the rejection of dependent claim 8 under 35 U.S.C. §103(a) as being unpatentable by *Burstein* is therefore respectfully requested.

E. Claims 3-7, 11 and 14 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim

The Applicant has added an independent claim 18 herein directed to the allowable subject matter of claim 3. Therefore, the Applicant respectfully requests an allowance of claim 18 over the art of record.

F. Claim 9 was objected to as being dependent upon a rejected base claim, but would be allowable if rewritten to overcome the 35 U.S.C. §112, ¶2 rejection

The Applicant has added an independent claim 19 herein directed to the allowable subject matter of claim 9. The Applicant has further added a claim 20 depending from claim 19 and directed to the allowable subject matter of claim 3. Therefore, the Applicant respectfully requests an allowance of claims 19 and 20 over the art of record.

SUMMARY

Examiner Tran's 35 U.S.C. §112 rejection of claims 9 and 15 has been obviated by the amendment to claims 9 and 15. Examiner Tran's objection of claim 15 has been obviated by the amendment to claim 15. Examiner Tran's 35 U.S.C. §102 rejection of claims 1, 2, 10, 12 and 13 have been obviated by the above remarks. The Applicant respectfully submits that claims 1-20 fully satisfy the requirements of 35 U.S.C. §§ 102, 103 and 112. In view of the foregoing, favorable consideration and early passage to issue of the present application is respectfully requested.

Dated: **September 5, 2002**

Respectfully submitted,
ZHENHUA WANG

U.S. PHILIPS
580 White Plains Road
Tarrytown, New York 10591
Phone: (914) 333-9606
Fax: (914) 332-0615

Jack D. Slobod
Registration No. 26,236
Attorney for Applicant

CARDINAL LAW GROUP
Suite 2000
1603 Orrington Avenue
Evanston, Illinois 60201
Phone: (847) 905-7111
Fax: (847) 905-7113

Frank C. Nicholas
Registration No. 33,983
Attorney for Applicant

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Claims 1-15 have been amended as follows:

1. (Amended) [Voltage] A voltage level monitoring circuit, comprising:

[-] a first reference current source (5) for generating a first reference current (I_{ref1});

[-] a monitoring current source (4) for generating a monitoring current (I_M) derived from a voltage (V_M) to be measured; and

[-] a comparator device (10) [comprising] including a first current input (11) coupled for receiving the first reference current (I_{ref1}), [and] a second current input (12) coupled for receiving the monitoring current (I_M), and at least one measuring signal output (13),

[the] wherein said comparator [being] is arranged for comparing the currents received at its two current inputs (11, 12) and for generating at the measuring signal output (13) a measuring signal (S) with a first value when the current received at its second current input (12) is less than the current received at its first current input (11), and with a second value when the current received at its second current input (12) is more than the current received at its first current input (11).

2. (Amended) [Voltage] The voltage level monitoring circuit according to claim 1, wherein the first reference current source (5) [comprises] includes a PMOS transistor (50) having its source coupled for receiving the voltage (V_{DD}) to be measured, having its gate coupled for receiving a bias voltage (V_{bias}), and having its drain coupled to the first current input (11) of the comparator device (10).

3. (Twice Amended) [Voltage] The voltage level monitoring circuit according to claim 1, further comprising:

a second reference current source (6) for generating a second reference current (I_{ref2}), a current output of the second reference current source (6) being coupled to the comparator device (10) through a controllable switch (7).

4. (Amended) [Voltage] The voltage level monitoring circuit according to claim 3, wherein the controllable switch (7) is controlled by a control signal (Sc) generated by the comparator device (10).

5. (Amended) [Voltage] The voltage level monitoring circuit according to claim 4, wherein the control signal (Sc) renders the controllable switch (7) conductive when the magnitude of the current received at the first input (11) of the comparator device (10) is higher than the magnitude of the current received at the second input (12) of the comparator device (10), and renders the controllable switch (7) non-conductive when the magnitude of the current received at the first input (11) of the comparator device (10) is lower than the magnitude of the current received at the second input (12) of the comparator device (10).

6. (Twice Amended) [Voltage] The voltage level monitoring circuit according to claim 3,[,] wherein the second reference current source (6) [comprises] includes a PMOS transistor (60) having its source coupled for receiving the voltage (V_{DD}) to be measured, having its gate coupled for receiving a bias voltage (V_{bias}), and having its drain coupled to the controllable switch (7).

7. (Twice Amended) [Voltage] The voltage level monitoring circuit according to claim 3,[,] wherein the controllable switch (7) [comprises] includes a PMOS transistor (70) having its source coupled the current output of the second reference current source (6), having its drain coupled to the first current input (11) of the comparator device (10), and having its gate coupled to a control output (14) of the comparator device (10).

8. (Twice Amended) [Voltage] The voltage level monitoring circuit according to claim [1] 7, wherein the comparator device (10) [comprises] includes:

a first inverter (80) having an input (81) and an output (82); and

a second inverter (83) having an input (84) and an output (85)[;],

wherein the output (85) of the second inverter (83) [being] is connected to the output (13) of the comparator device (10) [;], the input (84) of the second inverter (83) [being] is coupled to the output (82) of the first inverter (80) [;], and the input (81) of the first inverter (80) [being] is coupled to both the first and second current inputs (11; 12) of the comparator device (10).

9. (Amended) [Voltage] The voltage level monitoring circuit according to claim 8, [as far as depending on claim 7,] wherein the output (82) of the first inverter (80) is coupled to the control output (14) of the comparator device (10).

10. (Twice Amended) [Voltage] The voltage level monitoring circuit according to claim 1,[,] wherein the monitoring current source (4) [comprises] includes:

a primary current source (41) for generating a primary current (I_P)[,];

a secondary current source (42) for generating the monitoring current (I_M) [,]; and

a process sensitive resistor (49) connected in series with said primary current source (41).

11. (Amended) [Voltage] The voltage level monitoring circuit according to claim 10, wherein the primary current source (41) [comprises] includes a PMOS transistor having its source connected to the voltage (V_{DD}) to be monitored, having its gate coupled for receiving a bias voltage (V_{bias}), and having its drain connected to a first terminal of the process sensitive resistor (49).

12. (Twice Amended) [Voltage] The voltage level monitoring circuit according to claim 10, wherein the secondary current source (42) [comprises] includes:

a first NMOS transistor having its source connected to ground and its drain coupled to the second current input (12) of the comparator device (10); and

a second NMOS transistor (44) having its source connected to ground and its drain connected to a [resisitive] resistive block (43) of the process sensitive resistor (49)[;],

wherein the gates of the first and second NMOS transistors (42; 44) [being] are connected together and to the drain of the second NMOS transistor (44).

13. (Amended) [Voltage] The voltage level monitoring circuit according to claim 10, [11 or 12,] wherein the process sensitive resistor (49) [comprises] includes a further PMOS transistor (46) having its gate terminal connected to its drain terminal in a gate/drain node and having its source terminal coupled to the current output of the primary current source (41) for receiving the primary current (I_P).

14. (Amended) [Voltage] The voltage level monitoring circuit according to claim 13, the process sensitive resistor (49) further [comprising] includes at least one combination of two cascaded transistors (PMOS 47, NMOS 48) connected in series with said gate/drain node, a first one of said cascaded transistors (47) having its source terminal coupled to the drain terminal of the further PMOS transistor (46), a second one of said cascaded transistors (48) having drain terminal connected to the drain terminal of said first one of said cascaded transistors (47), and the gate terminals of said cascaded transistors (47, 48) being connected to each other and to the respective drain terminals of said cascaded transistors (47, 48).

15. (Amended) [Voltage] The voltage level monitoring circuit according to [any of the previous claims] claim 1, wherein [any of] the monitoring current source (4)[, the first reference current source (5), and the second reference current source (6) comprises] includes a programmable current source (90).